DELIVERABLE REPORT

JU Grant Agreement number: 737487

SILENSE

“(Ultra)Sound Interfaces and Low Energy iNtegrated SEnsors”

Test & Validation Concept Paper

Deliverable Report for D 3.4.1

Due Date: M15 – 2018-07-31

Point of Contact

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Nature:	**"R = Report"**		
Dissemination Level:	**PU**	Public	X
	PP	Restricted to other program participants (including the JU)	
	RE	Restricted to a group specified by the consortium (including the JU)	
	CO	Confidential, only for members of the consortium (including the JU)	

Project Information			
Work package		WP 3	Electronics
Task		T 3.4.1	
Deliverable		D 3.4.1	Test & Validation Concept Paper
Lead Contractors	**Work package**	IFAT, Alessandro Caspani	
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Executive summary
This document is the presentation of the test and validation methodology and objectives for each of the blocks/systems developed in the scope of the SILENSE project. Different test and validation level are presented: analog building blocks, digital building blocks or FPGA and lastly at the full system level. The responsible for the test are indicated for each building block in order to facilitate some exchange between partners on this topic. It shows that the elaboration of the test and validation procedure is not at the same progression level. The proposed document will be therefore helpful to sensitize the partners to the validation issue and will promote the exchange on this topic.

Date	Version	Author	Comments

2018-06-14	0.1	Dominique Morche	1st draft/template to request input from partners
2018-06-30	1.0	Dominique Morche	1st compilation of initial contributors
2018-09-15	2.0	Dominique Morche	Assembling of all contribution for review
2018-10-31	3.0	Dominique Morche	Revision after review

TABLE OF CONTENT

1 INTRODUCTION

This document is the presentation of the test and validation methodology and objectives for each of the blocks/systems developed in the scope of the SILENSE project.
Different test and validation level are presented: analog building blocks, digital building blocks or FPGA and lastly at the full system level. The responsible for the test are indicated for each building block in order to facilitate some exchange between partners on this topic. It shows that the elaboration of the test and validation procedure is not at the same progression level. The proposed document will be therefore helpful to sensitize the partners to the validation issue and will promote the exchange on this topic.

2 ANALOG CIRCUITS

This first part gives an overview of the tests method which will be applied to the analog building blocks specifically developed in the project.

- IMEC will no longer manufacture low power CMOS ADCs but will rather focuses on low power amplification on flexible substrates. In the scope of (WP2) IMEC is working on flexible transducer technologies, however in this work package, IMEC will contribute to investigate the direct use of thin-film transistor technologies on flexible substrates for driving and readout of transducer technologies. As such, it is expected to improve on key parameters as an improved SNR or to move towards the readout of larger matrices. The test of this devices will therefore be achieved simultaneously with the whole system.
- CEA-LETI will develop analog IC. Among those blocks a sigma-delta modulator will be developed whose characterization is different from classical ADC. The objective will be to reduce the power consumption of such system whose characteristics are particularly adapted to high resolution as well as digital beamforming.
  The architecture is still under investigation but a second order modulator, whose architecture is described in Figure 1 appears to be an interesting solution. Firstly, because of the robust stability of the architecture which will allows to introduce some tunability in the ADC and secondly it can be improved by adding a noise cancelling loop to emphasize the noise shaping with a limited impact on the power consumption.

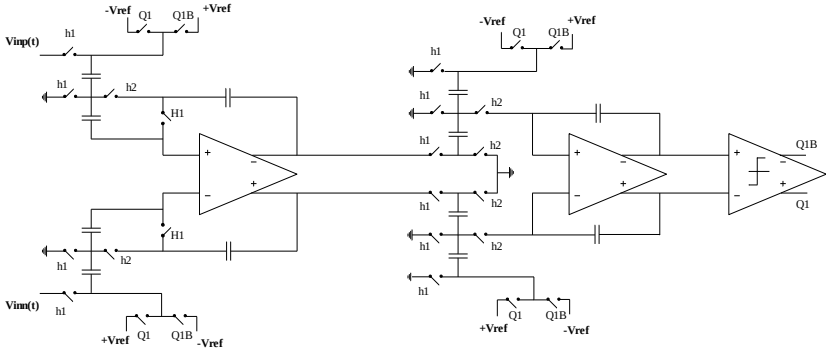

Figure 1: Switched capacitor architecture of the second order modulator

The envisioned list of pads of the device and their signification is given in Table 1.

Table 1 : List of pads

NAME	FUNCTION	REMARKS/VALUE
VDD, VSS	Power Supply	1.2V (+/- 10%)
PVREF,MVREF	Positive, Negative Voltage Reference	Tunable
AGND	Analog ground	0.6 V
B1	Input Bias	TBC
ENN,ENP	Negative, Positive Input Signal	0.5V peak

PD	Power Down	Active at “1”
CK	Clock Input	TBC
Q1,Q2	Output of the first (second) modulator	-
MOD	Functioning Mode of the modulator	“1” “0”
LEVP,LEVM	Add .Positive, Negative threshold	TBC

- Characterization system

Two test methods will be used to test the analog modulator. They are presented in Figure 2. The first one uses a classical signal generator. The input is applied to the device under test and after digital filtering and high precision digital to analog conversion, the signal is observed by using a spectrum analyzer.
The second method uses a synchronous signal generator with a high resolution D to A converter. A data acquisition board that will be developed internally will then be used to capture the signal output. Then the same tools that have been used for the design of the modulator can analyze the data. By this way, some signal processing can be used to deeply analyze the limiting factors of the analog modulator.

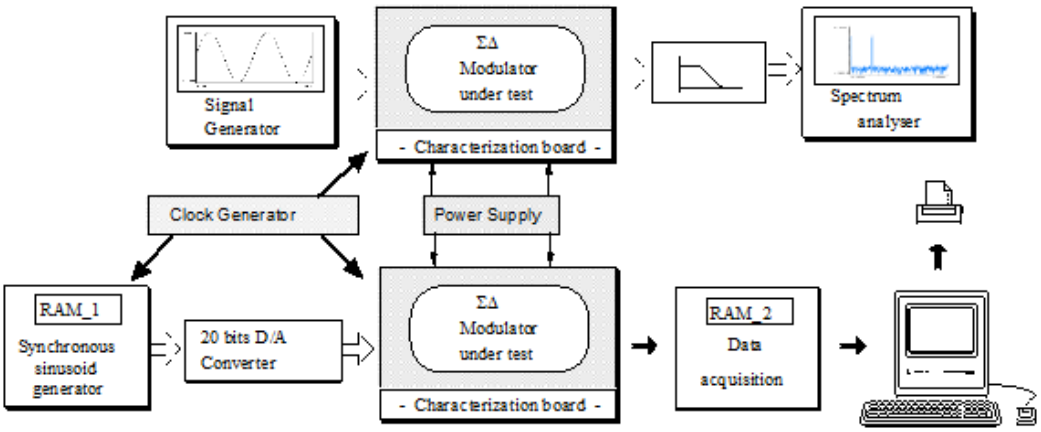

Figure 2: Synoptic of the characterization system

The characterization technique will focus on the main following parameters:

- Signal to Noise Ratio (SNR)
- Signal to Noise plus Distorsion Ratio (SNDR)
- Spurious Free Dynamic Range (SFDR)
- Total Harmonic Distorsion (THD)
- Power consumption vs uses cases
- Bandwidth
- Power Supply Rejection Rate (PSRR)

An automation of the characterization procedure will be developed to facilitate the test of an important number of components.

3 DIGITAL CIRCUITS AND FPGA

The digital circuit and fpga being much closer to the demonstrator level, the associated characterization include more high level system level.

3.1 NATIONAL INSTRUMENT BASED TESTING

BCB will implement their LabVIEW code on a National Instrument (NI) Industrial Controller to digital signal validation and proper communication with the Electronic Control Unit (ECU) of the vehicle via CAN bus.

3.2 US MICROPHONE ARRAY AND CHIRP GENERATOR, TESTING

UTIA plans to implement ultrasound (US) based gesture detection. For that purpose we have implemented prototype platform based on Xilinx Zynq7000 family industrial board (we use Trenz TE0720 SoM attached to either HDMI video capable TE0701 or smaller format TE0706). The board is connected via driving/controlling electronic circuit to prototype US microphone array. Before several different algorithm candidates can be used for gesture detection we propose setup shown in Figure 3 to test the performance of all system components.

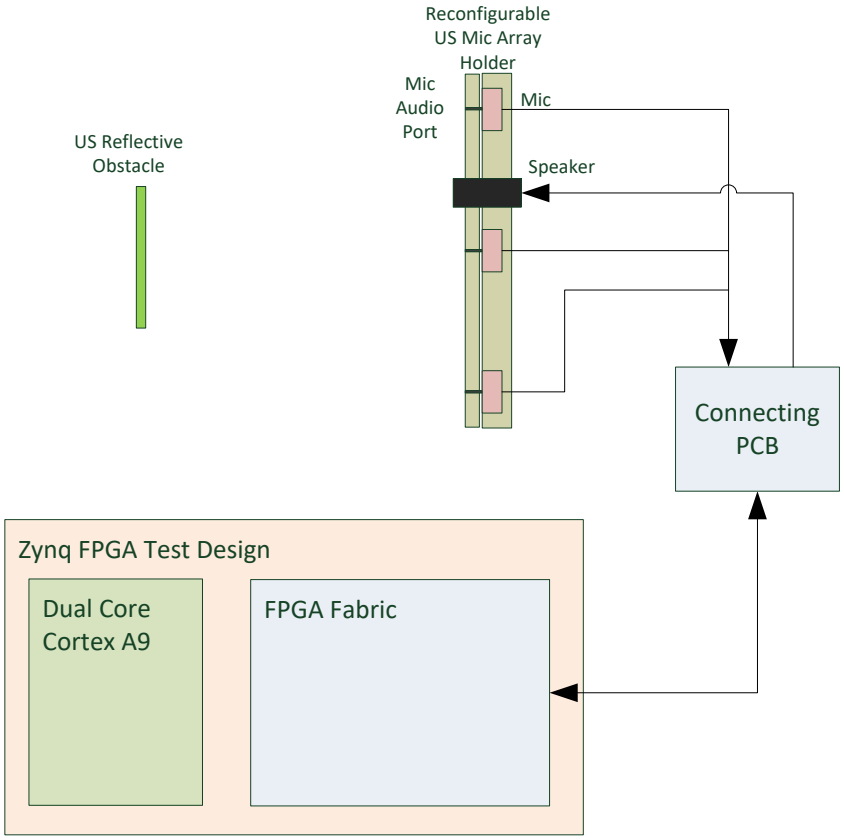

Figure 3: Microphone array test configuration

Key part of the setup is a Reconfigurable US microphone array holder – flat 3D printed board holding US capable microphones in precise distances. It also allows US speaker to be positioned. The holder is connected to Zynq FPGA module via Connecting PCB to FPGA I/O pins. The FPGA fabric provides all control to US speaker and also to microphones. An US reflective obstacle is placed at defined distance from the holder. The holder allows positioning of up to 9 microphone kits on flexible cables to three different organisations. The first is 3x3 rectangular array with microphone distance 40 mm. The second is 9 microphones in linear organization with minimal possible distance. The third is circular organization of 3 microphones placed at minial possible mutual distance. The minimal distance comes from physical dimension of used microphone kit. The holder design is shown in Figure 4. Microphone kit is supposed to be placed on top of the holder with its audio port facing up. Wires then go throught the rectangular hole to bottom side of the holder where Connecting PCM can be located.

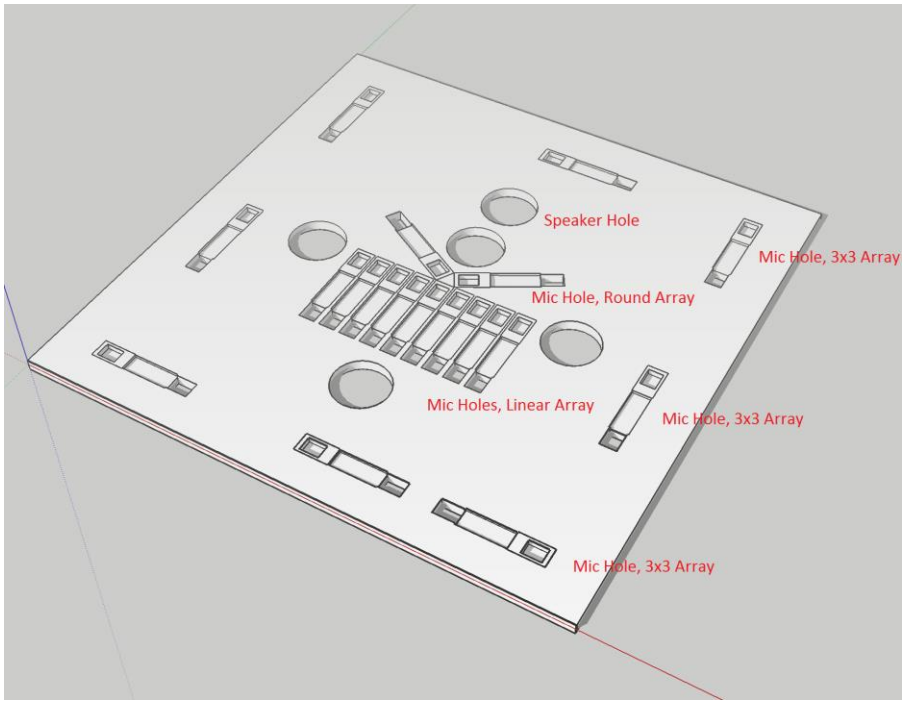

Figure 4: The reconfigurable microphone array holder - 3D printed model.

The baseline design for FPGA was implemented in Vivado, see Figure 5. The design contains interfaces for microphone array and for generating chirp waveform. The design is exported as a platform for Xilinx SDSoC 2017.4 tool. In the SDSoC we have provided simple C++ coded hardware accelerators capable to generate chirp waveforms and recording their echoes at the same time. In addition we have implemented decimation accelerator which will be able together with ACF and beamformer accelerators to provide support for gesture detection. The form of SDSoC platform provides possibility to quickly implement and test the HW accelerators using Vivado HLS tool and adapt them flexibly to our needs. The dual core ARM Cortex A9 is used to run Linux. The SDSoC tool implements user applications capable to use the accelerators, generate chirps and capture mic array data. It also supports writing captured data to filesystem where it can be accessed via standard FTP or by other means.

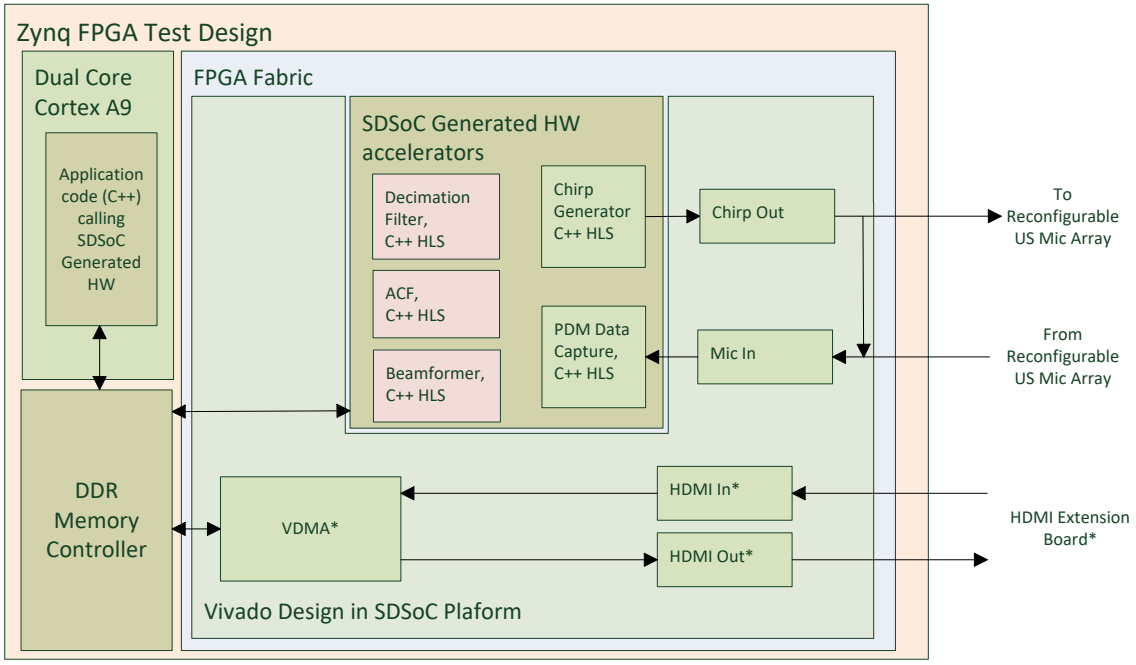

Figure 5: Zynq FPGA design used for testing microphone array.
*Only present if carrier TE0701 is used.

The described test setup can be used for:

- Testing performance of array holder assembly
  We can test if microphone ports are not obstructed and can receive undistorted waveforms. The organization of individual microphones in array must be also verified.
- The optimal chirp waveforms
  The chirp generator can be used to generate parametrizable chirp. We assume the different chirp length, FM coded chirps or use of barker codes for start. We would like to see how used speaker is capable to follow generated waveform and what is the influence of the chirp to the precision of echo detection. The influence of driving electronic to the quality of the chirp can be also observed.
- Check different microphone array geometry
  We would like to test also different microphone organisations – 3x3 array, 9 linear, 3 circular or any other by 3D printing new microphone array pattern.
- HW Accelerator development and testing
  As the data from microphones are captured and transmitted to PC the algorithms for gesture recognition can be developed and benchmarked. For their implementation in the embedded hardware we can use our SDSoC design as a starting point to develop efficient hardware acceleration for real-time gesture recognition.

We provide simple source code example how the system for chirp generation and microphone data capture can be implemented for our SDSoC tool platform. The example implements simple single chirp generation and capture in form of command-line executable with parameters. The application can be used as a starter for development of more complex chirp generation or custom DSP accelerators development. The example of simple chirp and

its measured shape captured by the example application can be seen in Figure 6. The bottom waveform is generated chirp. Top graph shows captured data synchronized to chirp time. The chirp changes its phase once in the middle. The captured waveform shows how our resonator-based speaker reacts to the phase change in the middle of the chirp (around time 200). The echo of the chirp can also be seen around time 400.

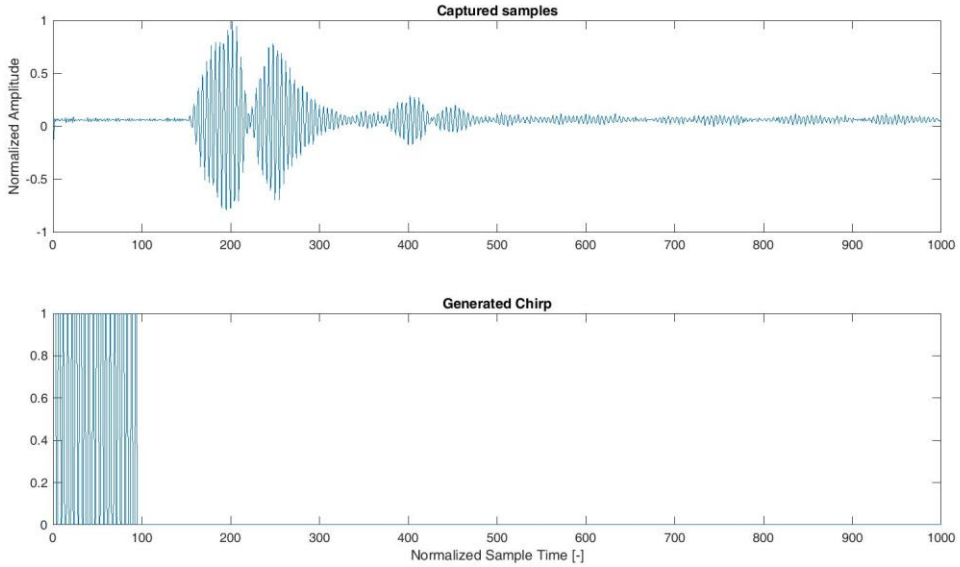

Figure 6: PCM samples captured by one microphone (top) and generated chirp waveform (bottom). Synchronous sampling rate at 192 kHz. Chirp frequency 40 kHz. In the middle of the chirp is phase reversed. Top waveform shows phase reversal in chirp and as well in chirp echo.

3.3 IMA PROVIDING US-READER HARDWARE FOR DEMO4

3.3.1 VALIDATION ENVIRONMENT

IMA is in charge of Smart access control demonstrator (Demo 4) and in this respect IMA will approach to validation process in order to show up if the US components work in compliance with requirements set up in work package 1.

For the validation process we need to install and set up full IMAporter platform because the gesture detected has to be verified if it matches with the one enrolled in the IMAporter system.

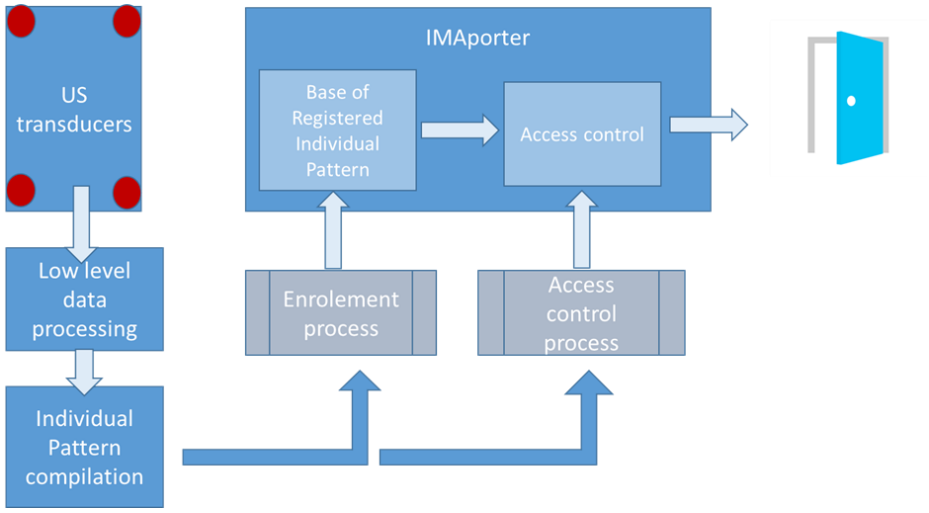

Figure 7: *IMAporter access control platform*

- **Gesture reader**

In the DEMO4 the reader is innovated with communication protocol receiving gesture data from ultrasonic sensor. The data are processes in order to get individual pattern of users. Patterns are processed either in enrollment session or standard access control check out session.
Gesture reader will be the main part of the validation process.

Figure 8 : *RSW.04Ges*

- **Ultrasonic sensors, transducers (UTIA, BUT)**

The component will be provided by partners UTIA, BUT. A specific verification procedure will be established in collaboration with these partners.

- **Data processor (UTIA, BUT)**

The component will be provided be partners UTIA, BUT. A specific verification procedure will be established in collaboration with these partners.

- **Communication terminal CKP**

This component is standard part of IMAporter, will run standard functionalities, configured to communicate with RSW.04Ges in standard mode. As a standard component, no specific validation is needed.

- **Data master K4Master**

This component is standard part of IMAporter, will run standard functionalities, configured to communicate with RSW.04Ges in standard mode. As a standard component, no specific validation is needed.

- **K4 database, K4 Server**

This component is standard part of IMAporter, will run standard functionalities, configured to communicate with RSW.04Ges in standard mode. As a standard component, no specific validation is needed.

- **Application K4Manager**

The application is in charge of

- entities management
- readers management
- access rights management
- network communication management

In order to pass validation process, the application will be properly configured.

3.3.2 VALIDATION PHASES AND TEST PLAN

The demonstration will be considered as successful as a whole if following functions and aspects will be tested and running properly fulfilling defined requirements:

- ✓ All components are inter-connected and no error reported after installation
- ✓ Gestures of persons involved are successfully enrolled and stored in the system
- ✓ Management of the gesture (person assigned, time validity, reader assignment)
- ✓ Gesture is successfully detected at the reader and system matches the gesture with database, gate is unlocked
- ✓ Gesture is successfully detected at the reader but system does not find any gesture in database, gate is not unlocked
- ✓ Rating of valid gesture/unlocked gate : valid gesture/locked gate is 10:1 (success rate can be reconsidered according to any update of the demonstrator target)
- ✓ Rating of invalid gesture/locked gate : invalid gesture/unlocked gate is 100 :1 (success rate can be reconsidered according to any update of the demonstrator target)

Validation process will be focused on functional performance of the reader RSW.04Ges. The functional performance will involve tests & test results given in following Table 2.

Table 2: Functional Performance

Test name	Expected test result (NA in this deliverable)	Result w.r.t. criteria (NA in this deliverable)
Reader (IMA) establishes communication with gesture detector (UTIA, BUT)		

Reader receives data package characterizes a gesture.		
Reader sends verification request to CKP terminal		
Reader receives respond from CKP terminal		
CKP terminal takes request/respond session in order to verify gesture validity (gesture stored or not in database)		
CKP takes the open/close action		
Application message log to check		

3.3.3 VALIDATION CRITERIA

Validation criteria w.r.t. use case requirements will be simplified and focused on demonstrator function performance. Criteria selected are shown in the Table 3

Table 3:Selected Criteria

C1	Communication lower protocol consists of defined data (protocol spec)	Y/N
C2	System component reaction	Action/Fail/Error/System stuck
C3	UI appearance	Expected Y/N/Deviation
C4	Message content in Application log	Expected Y/N/Deviation

- SNPS will prototype low-power, high performance embedded processors on FPGA board (EM Starter Kit development platform)

4 SYSTEMS (ANALOG & PROCESSOR)

- CTR will provide application test boards

4.1 CMUTS CHARACTERIZATION

4.1.1 CHAMBER STRUCTURE

For the characterisation of the cMuts from Infineon, CTR is designing and building an "Anechoic Ultrasound Chamber". Inside the measurement chamber a variable positioning system will be located which allows for automated measurements.

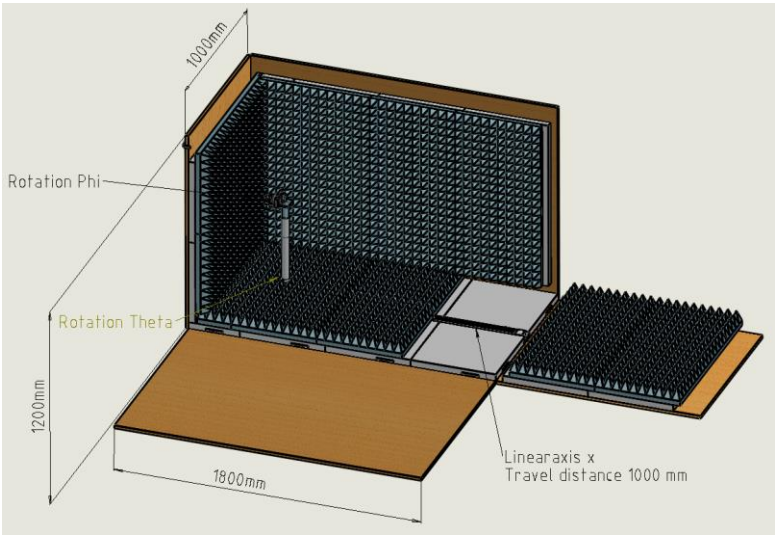

Figure 9: Anechoic Ultrasonic Chamber Overview

The Chamber consists of a wooden case with the dimensions 1200mm x 1000mm x 1800mm (see Figure 9). To enable easy access to the inside of the measurement chamber the upper, right and the front panels can be opened. To insulate the chamber from vibrations coming from the building floor the box will be standing on 6 rubber vibration buffers. Four different absorber materials will be installed on the inside of the panels to insulate the measurement chamber from acoustic noise from outside of the measuring chamber and to minimize reflections inside the chamber (see Figure 10).

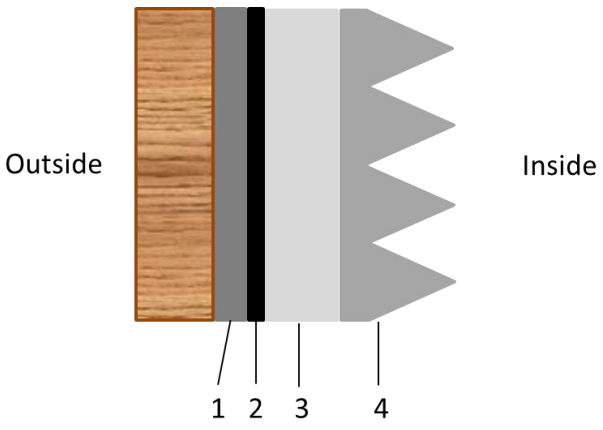

Figure 10: Absorber stack section view

The different materials in the stack have been chosen to attenuate the frequency band from 20 kHz to 150 kHz. In a preliminary validation different foam materials were evaluated. The chosen material and are listed in Table 4 and their position in the absorber stack are shown in Figure 10.

Table 4: absorber materials

Position	*Materialdescription*
1	High quality planner foam [MicroPor] 10 mm
2	Bitumen heavy foil [Bitufolie2SK]
3	Sound insulation foam ester [AV40G/AV50G] 40 mm/50 mm
4	Pyramid foam [BPyrG70] 70mm

4.1.2 MECHANICAL SETUP

For the realization of an angle and distance dependent characterization three types of actuators are necessary. To get a variation of the spacing between the speaker and the microphone a linear stage will be installed. The distance between the measurement microphone and the sample under evaluation can be varied from 0 mm to 1000 mm with an accuracy of ~1 mm.
Rotation stages are used to rotate the transducer around the z-axis and the x-axis. This makes it possible to characterize the transducer in a range of ±90 degrees. The repeatability for θ and φ is ~< 0,5°. In Figure 11 the orientation of the linear stage and the rotation axis are shown.

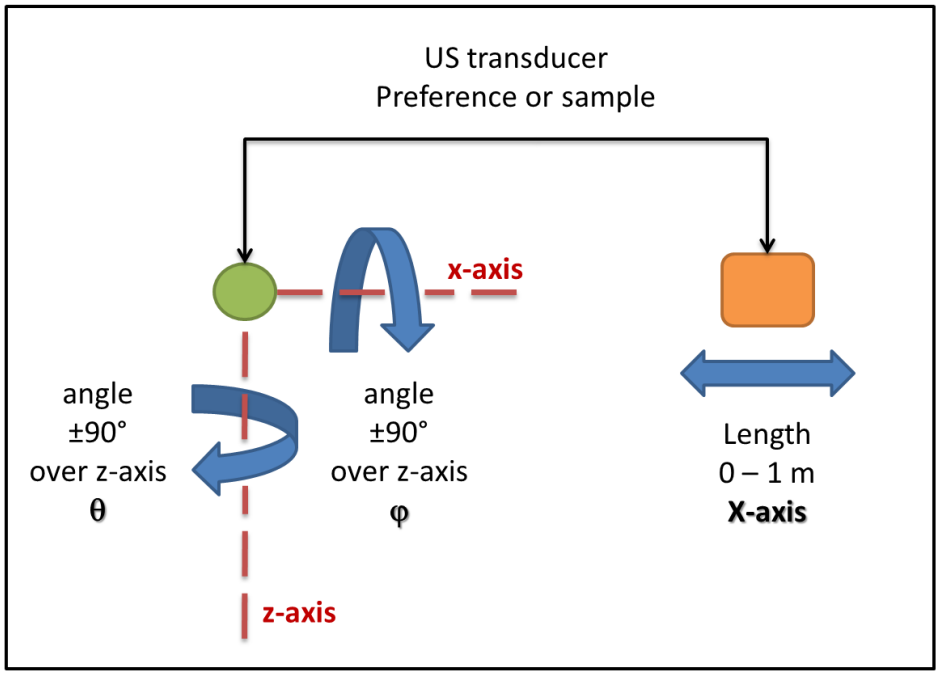

Figure 11 : angle and distance dependent positioning

To ensure that the received signals come from the transducer and are not reflections from the absorber material, the speaker and the microphone were placed, on posts with a height of 1 m, in the middle of the measurement chamber.

4.1.3 ELECTRICAL SETUP

To automate the measurement and for the generation and acquisition of the data, the following equipment will be used:

Table 5 : electric equipment list

Amount	Device Name	Description
1	PH520-4810	48 V power supply for driving the stepper motors
1	6EP1 336-3BA00	24 V power supply for the motor drivers, encoder and other equipment.
3	IDS240-5EI	Motor controller for the 3 stepper motors (x,θ and φ)
1	PC	PC is used to control the motors, generate the input signals and store the measured data.
1	ArbStudio 1104	Waveform generator for input signal.
1	604142	Series 600 instrument grade ultrasonic sensor to calibrate the A.U.C. as speaker
1	G.R.A.S 14 AA	Amplifier for the input signal of the speaker (604142 only)
1	G.R.A.S 40DP	1/8” pressure microphone for characterisation of the speaker
1	G.R.A.S Type 12AK	Electrostatic actuator amplifier for the microphone
1	Wavepro 725zi	Oscilloscope to read the amplified data from the microphone

4.1.4 MEASUREMENT SETUP

Before characterising the cMuts transducer as speaker, the “Anechoic Ultrasound Chamber” has to be calibrated. For the calibration we will use the Series 600 Instrument Grade Transducer from the company SensCom as speaker. The generation of the signals are done by a LabView program and send to a waveform generator. The signals were amplified by an electrostatic actuator amplifier for the speaker input. The acoustic output form the speaker will be recorded by the microphone and amplified by the power module. To record and to visualize the data, an oscilloscope will be used.
After the calibration step, the transducer will be measured using the same procedure. For the signal generation, the amplifier has to be adapted.

The measurements were made with the following parameters:

- Frequency 20 kHz to 150 kHz (Different signal ramping is possible (active damping etc.)
- Distance between speaker and microphone will be variated: 0 – 1 m (X-axis)
- Angular Directionality of the speaker will be variated: 180 Deg. φ and θ

As description of the measurement sequence a simple state machine diagram is shown in Figure 12.

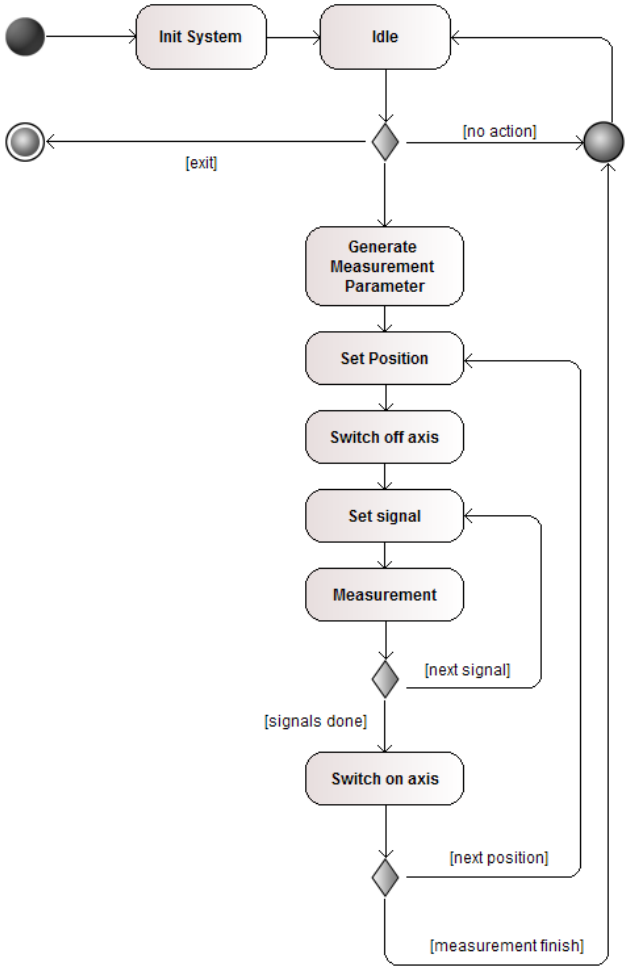

Figure 12 : state machine diagram of characterization measurement

4.2 SYSTEM CHARACTERIZATION

NXP Fr. and NXP Nl will develop test benches for testing haptics and ultrasound features. The following test benches will be developed:

- Test bench for testing a driver for haptic patterns. The test bench will comprise an amplifier including DSP for haptic pattern generation, a Linear Resonant Actuator, and an accelerometer to capture haptic feedback.
- Several ultrasound test benches:
  - Hardware test bench to evaluate intermodulation of ultrasound generated by a Class-D audio amplifier. Test bench will be able to detect distortion of audio band caused by ultrasound and vice versa
  - Algorithm test bench containing database of ultrasound recordings for development of ranging and gesture sensing algorithms
- Full system testbench comprising device mock-ups (e.g. mock-up phones, smart watches) containing haptic and ultrasound features for full system performance analysis

5 CONCLUSIONS

This document has shown the status of the test and validation activity which is still ongoing. It will be helpful to facilitate the exchange between the partners to finalize the concept and prepare the hardware part of the test environment.