DELIVERABLE REPORT

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SILENSE

“(Ultra)Sound Interfaces and Low Energy iNtegrated SEnsors”

Deliverable Report for D 3.2.1

Electronics concepts document

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Executive summary

This document gives a public overview of all hardware IP developments planned within WP3 of the Silense project.

Date	Version	Author	Comments
10/12/18	V1	Joost van Beek	First version, which is a public summary derived from D322
10/15/18	V2	Joost van Beek	Included comments from IFAT and CEA

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1.1 Introduction

This report gives a general overview of all hardware IP development planned for Silense. IPs described in this deliverable constitute the electronics hardware development needed for realizing final project demonstrators.

Section 1.2 describes the different IPs as being developed by the partners. Section 1.3 explains the relation of IPs developed by partners to the realization of the overall project demonstrators.

1.2 Individual IP blocks: general description

1.2.1 NXP-NL: Ultrasound generator & wireless ultrasound beacon

NXP-NL will develop hardware IP for gesture recognition, indoor navigation, echo-location, and device pairing. For the gesture recognition system, NXP will develop ultrasound generator IP integrated into an audio-amplifier IC for use in mobile phone. For the indoor navigation system, NXP will develop wireless beacons transmitting ultrasound signals that can be used for indoor navigation, echo-location, and device pairing

1.2.2 NXP-F/B: Haptic driver hardware for Linear Resonant Actuator

NXP-F and NXP-B will update Audio amplifier IP to drive Linear Resonant Actuator and support Haptic feature for Silense demonstrators.

1.2.3 IMEC: Towards amplification on flexible substrates

A route that IMEC pursues is to integrate monolithically a 2-D array of large area transducers together with a thin-film transistor technology as depicted in next figure. The thin-film transistors are also used as switches for the row-column addressing of the 2-D array.

1.2.4 SNPS: ARC EM Development System

SNPS will develop an ARC based development platform. The ARC EM Development System is an FPGA based prototyping system to demonstrate ARC based processor subsystems.

1.2.5 TUE: System for gesture and voice recognition

TU/e will develop a user-friendly setup of transducers consisting of duplicated units of mini-clusters which leads to the interpretation of Ultrasound activity in a form of an image. This is followed by machine learning algorithms to classify a set of gestures represented by the 2D transducers output.

1.2.6 CEA-LETI: Analog IP for the reduction of the power consumption

CEA-LETI main activity is in the development of new analog IP for the reduction of the power consumption. This is strategical to the ultra-sound detection since it is one of the most interesting features of ultrasound imaging and sonar.

1.2.7 IFAT: ASIC for interfacing the capacitive micromachined ultrasound transducers

IFAT will develop an ASIC for interfacing the capacitive micromachined ultrasound transducers (cMUT) developed by IFAG to the processing unit where the application specific algorithm is executed.

1.2.8 CTR: Anechoic Ultrasound Chamber for capacitive ultrasound transducer characterization

CTR will perform test measurements of the “Anechoic Ultrasound Chamber” with calibrated microphone and speaker over the frequency band from 20 kHz to 200 kHz. For the single measurement the distance, the vertical and the horizontal angle to the microphone were changed. Furthermore, the frequency and the form of the input signal are varied.

1.2.9 IMA: Access control reader, protocol with ultrasound detector

IMA will develop IP for an access control reader, incl. ultrasound detector protocol as required for Demo4.

1.3 Individual IP blocks: link to Project Demonstrators

Matrix description linking hardware IP blocks that are to be developed to realize project demonstrators is shown in Table 1.

Table 1: IP - Demonstrator matrix

	Demo1.1 Smart Acoustic Wearable System	**Demo1.2** Multi-purpose gesture recognition system	**Demo1.3** Touchless interaction & US infrastructure	**Demo1.4** Human motion tracking for sports and rehabilitation	**Demo3** Gesture recognition in smart home/ buildings	**Demo4** Smart access control	**Demo5** Automotive in-cabin gesture detection system	**D6** Underwater buddy system
NXP-NL	Ultrasound generator IP on Smart Audio Amp							
	Hardware assembly for wireless ultrasound beacon							
NXP-F	Haptic driver hardware for LRA							
NXP-B	Haptic driver firmware for LRA						.	
IMEC	In-pixel variable gain amplifiers on flexible substrates			ASIC for interfacing the capacitive micromachined US transducers will be relevant				pmuts for underwater localization simple but robust signal processing for underwater localization
TUE	Gesture and voice recognition engine							
CEA	Ultra Low power voice recognition engine							
IFAT		ASIC for capacitive ultrasound transducer	ASIC for capacitive ultrasound transducer				ASIC for capacitive ultrasound transducer to be integrated into interior part	
CTR		Anechoic Ultrasound Chamber for capacitive ultrasound transducer characterization						

IMA						Access control reader, protocol with ultrasound detector.		
SNPS					Hardware assembly for actuator driver firmware			